Variable-temperature, wafer-level capacitance measurements

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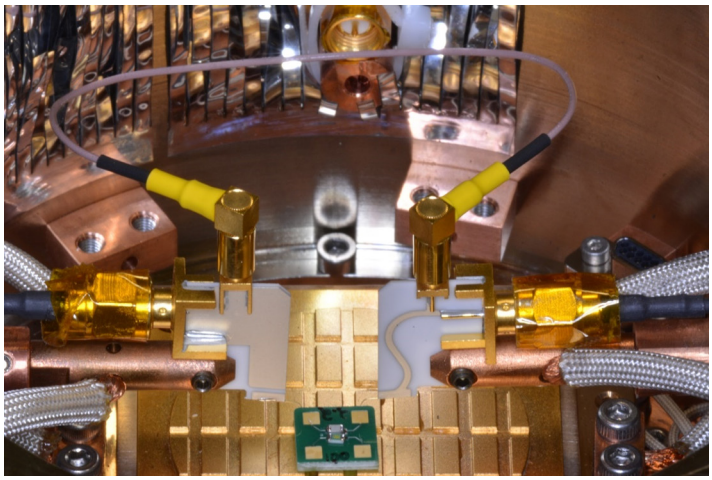

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Introduction

Wafer-level capacitance-voltage (or C-V) measurements assess of variety of semiconductor parameters on many material and device architectures including MOSFETs and MOS capacitors, while temperature-dependent C-V measurements can provide deeper insight into semiconductor growth quality, surface traps and carrier freeze-out [1].

Because of the utility of C-V measurements in characterizing emerging research grade devices, C-V measurements are often carried out at the wafer-level in a probe station; however, the offsets and drift in stray capacitance and residual inductance inherent in many probing geometries can mask key parameters derived from C-V measurements. Additional care is required in a cryogenic prober as these offsets can be temperature dependent. In this work, the techniques and instrumentational requirements for high-quality, wafer-level C-V measurements in a cryogenic probing environment are presented.

Experimental platform

Temperature-dependent C-V measurements were carried out in cryogenic (Lake Shore TTPX, CPX-VF) and cryogen-free (Lake Shore CRX-4K) probe stations using an auto-balancing, bridge-type C-V meter (MFCMU, Keysight B1500A). To achieve the best noise performance, the grounding lug of MFCMU was fastened to the probe station vacuum chamber. The probe stations were equipped with the Lake Shore C-V probe kit, which includes special dual-connector probes and cabling necessary to establish a shielded, two terminal (S-2T) configuration (Figure 1). The S-2T configuration ties together the shields of the two probes near the device and creates a current return path in the shield; this return current cancels the magnetic flux generated by the measurement. Without this return path current, the unmitigated magnetic flux will result in an increase in the residual cable inductance and can vary with the placement of the probes—reducing the overall accuracy of the capacitance measurement (Figure 2).

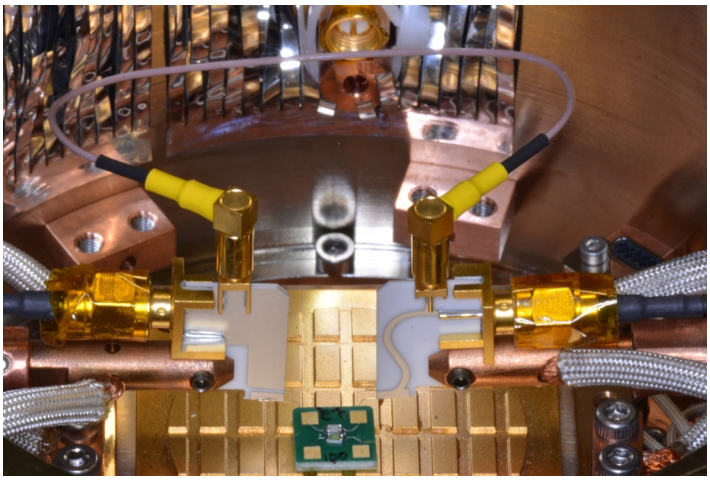

Figure 1. An S-2T configuration for C-V measurements is achieved with cryogenically-compatible parametric probes and a shorting cable, which ties the ground of each probe together. Probes and cable mounted in a TTPX cryogenic probe station.

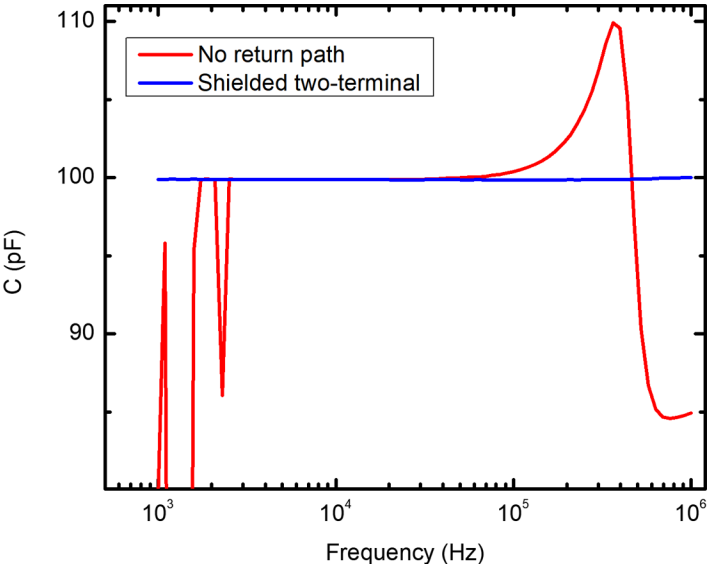

Figure 2. Measured capacitance of 100 pF device at 300 K using an S-2T configuration as well as a probing configuration without the shield return path.

The special dual-connector probes for C-V measurements are drop-in replacements for standard Lake Shore ZN50 probes. After mounting the probe blade, the standard signal cables are first connected to the SMA jack of both probes then the shorting cable is snapped-on the SSMB jacks on the probes. When installing the shorting cable, the probe arm should be supported from below to avoid forcing the probe tip into the sample holder. To prevent probe damage when removing the shorting cable, a small flathead screwdriver should be used to pry the shorting cable connectors from the probe jack (Figure 3).

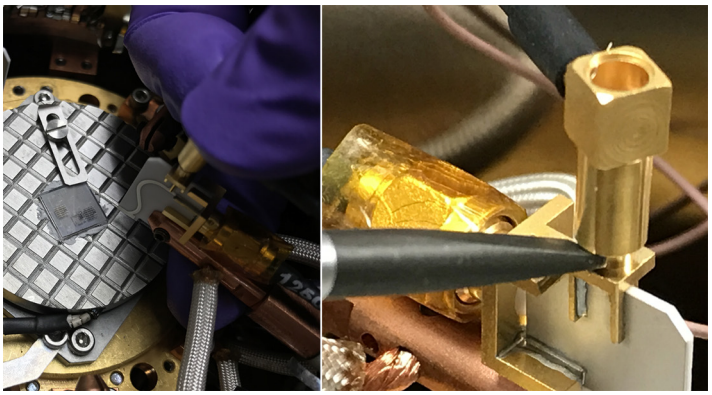

Figure 3. Installing (left) and removing (right) SSMB connector from the parametric probe.

In-situ cable compensation

In a probe station, the cables, probes, sample holder, and device can all contribute to the measured capacitance value. For measurements up to 1 MHz, an OPEN/SHORT compensation can often correct for the effect of the measurement platform. Details regarding the execution and storage of compensation data typically can be found in the manual for the C-V measurement instrumentation. For a SHORT compensation in a probing measurement, the two probes are navigated over the device under test (DUT) wafer and subsequently landed on the same contact pad. A non-negligible contact resistance between the probe and device can cause an error in the compensation and subsequently in the capacitance measurement. To minimize the contact resistance and contact resistance variability, particularly at cryogenic temperatures, tungsten probe tips should only be used on oxidizing contacts such as aluminum or refractory metals while gold-plated tungsten probe tips are available for use with softer device contacts especially those made of gold. To execute the OPEN compensation measurement, the probe should be lifted from the DUT wafer and separated by a distance equivalent to the device contact spacing. The quality of OPEN/SHORT compensation and the measurement noise can be assessed with a simple, post-compensation OPEN C-V measurement (Figure 4). Because the cable parameters change with temperature, an OPEN/SHORT compensation should be executed at each temperature in a thermal study.

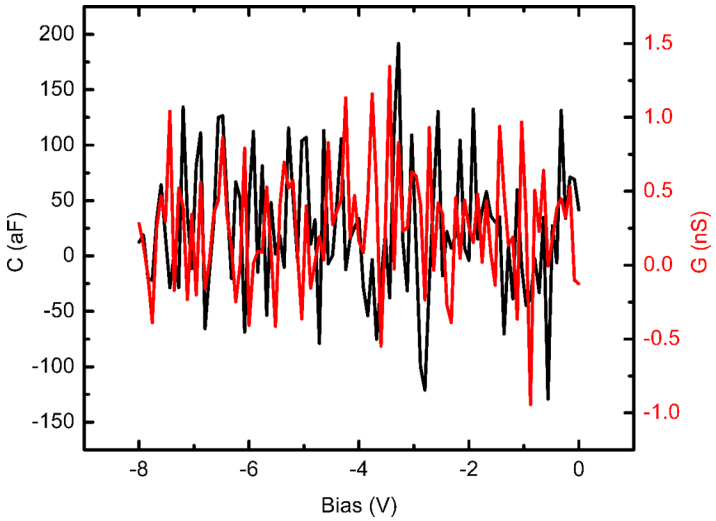

Figure 4. 100 kHz OPEN C-V measurement following cable compensation procedure. This measurement provides a measure of the inherent background capacitance as well as the calibration quality.

Temperature dependence of NP0-class capacitors

NP0-type capacitors require temperature coefficients less than ±30 ppm/K and a loss tangent below 0.001 for the temperatures between -55 and 125 °C. This stability is achieved by blending dielectric materials with both positive and negative temperature coefficients. Conventional NP0 ceramic formulations contain a significant proportion of neodymium, samarium and other rare earth oxides; blends of magnesium titanate and calcium titanate; or mixtures of neodymium carbonate, titania, and barium titanate [2]. Even though these capacitors are only rated for operation near ambient conditions, previous work has shown that certain commercially-available, NP0-type capacitors are well suited for cryogenic applications [3]. With an increasing need for cryogenically-rated microwave components such as multiplexers, the helium temperature performance of critical passive devices warrants further study. In the case of capacitors, ceramic formulations can vary with vendor as well as with regulatory and commodity conditions. Here we examine the cryogenic performance of two distinct compositions of commercially available NP0-type surface-mount capacitors.

Figure 5 shows the frequency-dependent capacitance (C-f) result from a precision 2.2 ±0.25 pF capacitor before and after the OPEN/SHORT calibration. Measurements were taken with a 2 V bias and a 50 mV oscillation. If measurements are particularly noisy, the oscillation amplitude and integration time can be increased to improve the performance of the current sensing electronics. The calibration procedure removes the high frequency tail as well as an offset. Once calibrated, the measured capacitance of this device shows minimal dispersion at elevated, ambient as well as cryogenic temperatures.

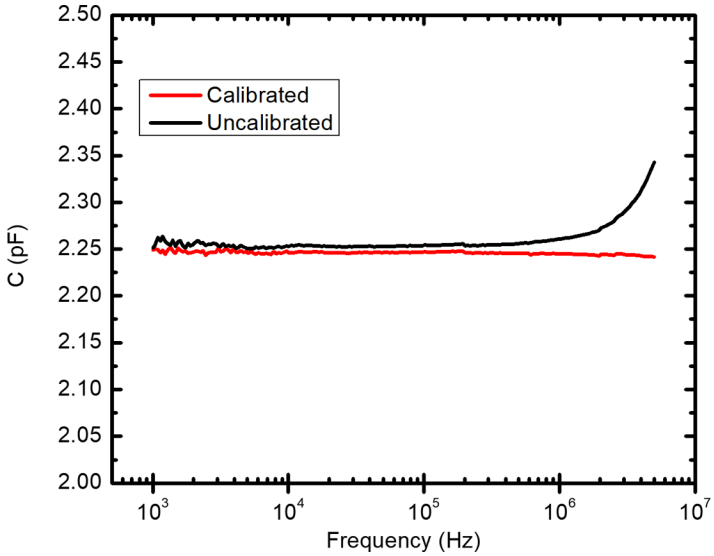

Figure 5. Calibrated and uncalibrated C-f measurement of a precision 2.2 pF capacitor at 300 K.

The capacitance of this same 2.2 pF capacitor was measured as a function of temperature. For this measurement, the stage of a CRX-4K probe station was set to a temperature between 5.5 K and 400 K. After reaching the set point temperature, the sample was "soaked" at temperature for 10 to 15 min to reach thermal equilibrium with the stage; the aforementioned SHORT/OPEN calibration procedure was carried out followed by a capacitance-voltage (C-V) sweep of the device. With a 30 mV oscillation, the device was swept from -10 V to +10 V and the average capacitance extracted from this data. Results are shown in Figure 6. From 300 to 400 K the capacitance of this NP0 device changes by +20 ppm/K and from 225 to 300 K the capacitance changes by -15 ppm/K—both well within specification. At temperatures below 200 K, the negative-positive ceramic compensation is less balanced and the overall capacitance of the device increases by ~1%. For many cryogenic applications, like filtering, this shift is sufficiently small.

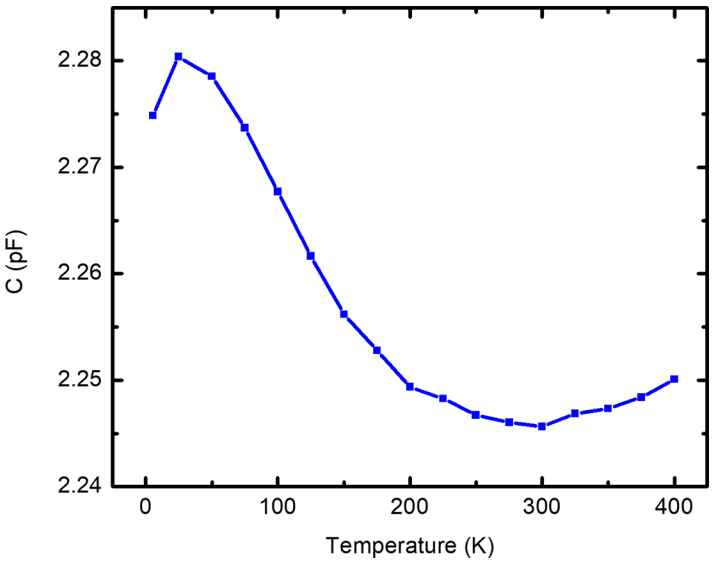

Figure 6. Temperature-dependent capacitance of a 2.2 pF NP0 device.

The second device was 5 nF multilayer capacitor composed of a low magnetic susceptibility ceramic. The 5 K, C-f measurement of this device is shown in Figure 7 with the capacitance extracted using parallel and series circuit models. As with any impedance measurement of a device, the result will include parasitic resistance, inductance and capacitance [4]. Effective circuit models are used to extract the device parameters from these parasitics. In the parallel circuit model with a capacitive device, the series resistance is assumed to be zero. In this case, the low temperature contact resistance (in series with the capacitor) and the high frequency impedance, $|Z|=1/\omega C$, are on the same order of magnitude. As a result, the error in the parallel capacitance model is quite large. As a rule of thumb for capacitance measurements, the parallel circuit model should be used for impedances above 10 kΩ where the series circuit model should be used for impedances below 10 Ω. For intermediate impedance values, care should be taken to characterize the contact resistance over temperature and compare the results from both equivalent circuit models.

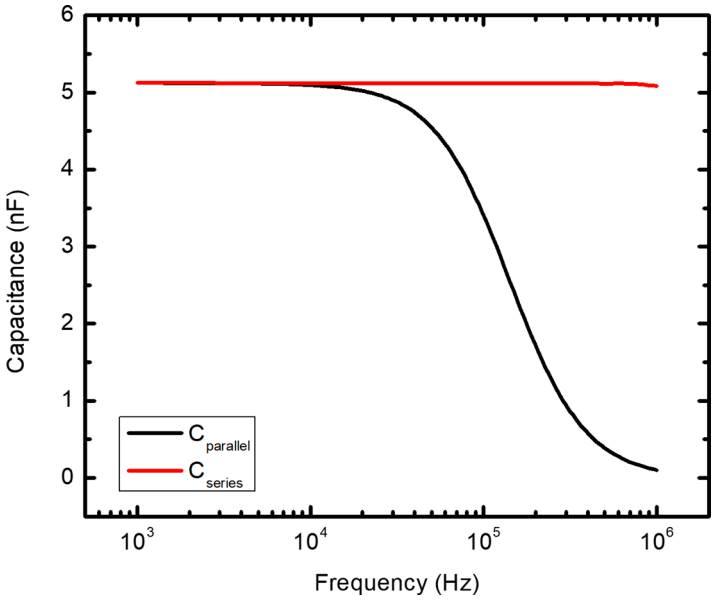

Figure 7. Comparing the equivalent circuit models in a C-f measurement of a 5 nF NP0 capacitor at 5 K. Low temperature contact resistance mandates the use of the parallel circuit model. At room temperature, both circuit models provide similar device parameters.

Conclusions

Here, wafer-level capacitance measurements are demonstrated using a cryogenic probe station. Dual-connector probes enable a cryogenically-compatible, shielded 2T wiring configuration; when coupled with in-situ calibration of the probing fixture and attention to the contact resistance, cryogenic characterization of wafer-level semiconductor and nanoscale devices is made possible.

References

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