Enhancement-Mode Antimonide Quantum-Well MOSFETs With High Electron Mobility and Gigahertz Small-Signal Switching Performance

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***Abstract*—This letter demonstrates, for the first time, enhancement-mode (e-mode) antimonide MOSFETs by integrating a composite high-κ gate stack (3 nm Al_2O_3 − 1 nm GaSb) with an ultrathin $InAs_{0.7}Sb_{0.3}$ quantum well (7.5 nm). The MOSFET exhibits record high electron drift mobility of 5200 $cm^2/V \cdot s$ at carrier density (N_s) of 1.8×10^{12} cm^{-2}, subthreshold slope of 150 mV/dec, I_{ON}/I_{OFF} ratio of ∼4000× within a voltage window of ∼1 V, high I_{ON} of 40 $\mu A/\mu m$ at V_{DS} of 0.5 V for a 5-μm gate length (L_G) device. The device exhibits excellent pinchoff in the output characteristics with no evidence of impact ionization enabled by enhanced quantization and e-mode operation. RF characterization allows extraction of the intrinsic device metrics (C_{gs}, C_{gd}, g_m, g_{ds}, v_{eff}, and f_t) and the parasitic resistive and capacitive elements limiting the short-channel device performance.**

***Index Terms*—Antimonide MOSFET, high-κ dielectric, InAsSb, low-power logic.**

I. Introduction

DEPLETION-MODE $InAs_{0.8}Sb_{0.2}$ quantum-well (QW) MOSFETs with high drive current have been already demonstrated [1], albeit with a degraded I_{ON}/I_{OFF} ratio due to the accumulation of holes in the barrier layer. The device is susceptible to the hole accumulation problem due to the very high conduction band offset between the $InAs_{0.8}Sb_{0.2}$ QW and the InAlSb barrier layer. For ultra-low-power logic devices, enhancement-mode (e-mode) operation is required along with high I_{ON} and I_{ON}/I_{OFF} ratio over a limited gate voltage swing. In this letter, we demonstrate $InAs_{0.7}Sb_{0.3}$ QW MOSFETs with a thin barrier and QW thickness, which exhibit e-mode operation due to stronger quantum confinement effects [2], [3]. As the QW is scaled, the subband energy levels in the QW will move up in energy, which gives rise to higher threshold voltage operation. The scaling of the InAlSb barrier layer prevents hole accumulation during device turnoff, resulting in a significantly improved I_{ON}/I_{OFF} ratio of 4000× at room temperature, which is a remarkable improvement over the previous generation thick QW device in [1], which had an I_{ON}/I_{OFF} ratio of only 30×. Record high long-channel electron mobility, short-channel electron velocity (after series resistance correction), and gigahertz domain small-signal performance are also demonstrated in these e-mode $InAs_{0.7}Sb_{0.3}$ QW MOSFETs, for the first time.

This letter is organized as follows. Section II describes the device layer design and characterization, Section III describes the dc and ac characteristics of the device, Section IV describes the RF characterization, and followed by conclusions in Section V.

II. Device Layer Design and Characterization

Fig. 1(a) shows the schematic of the QW device structure. The QW is undoped, and the $Al_{0.9}\,ln_{0.1}$ Sb barrier layer has been delta-doped with Te to provide carriers to the access regions. Fig. 1(b) shows the transmission electron microscopy (TEM) micrographs of the $InAs_{0.7}Sb_{0.3}$ QW FET stack grown on GaAs by molecular beam epitaxy and the defect-free active device layers. Fig. 1(c) shows the quantitative mobility spectrum analysis (QMSA) for the QW heterostructure obtained using magnetoconductance measurements at various temperatures and under varying magnetic field [4]. There is a single dominant conductivity peak due to electrons indicating no parasitic or parallel conduction through the barrier or the metamorphic buffer layers. We obtain a room-temperature Hall mobility value of 5500 $cm^2/V \cdot s$ ($N_s = 1.8 \times 10^{12}/cm^2$) for the QW heterostructure. Fig. 1(d) shows the top-view SEM image of the $InAs_{0.7}Sb_{0.3}$ MOS QW FET with 150 nm L_G and a composite high-κ gate stack (1 nm GaSb−3 nm Al_2O_3). A Pd/Pt/Au metal stack was alloyed to form embedded contacts making direct ohmic contact with the QW. Device isolation was done using Cl_2/Ar-based reactive ion etching followed by 3-nm-thick Al_2O_3 deposition employing plasma-enhanced atomic layer deposition [5]. The device layers were treated in HCl ($1HCl : 1H_2O$) for 30 s prior to gate dielectric deposition. A Pd/Au gate metal was defined using e-beam lithography and

Manuscript received September 15, 2011; accepted September 22, 2011. Date of publication October 26, 2011; date of current version November 23, 2011. This work was supported by the Focus Center Research Program for Materials, Structures, and Devices sponsored by the Semiconductor Research Corporation and the Defense Advanced Research Projects Agency. The review of this letter was arranged by Editor G. Meneghesso.

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Digital Object Identifier 10.1109/LED.2011.2170550

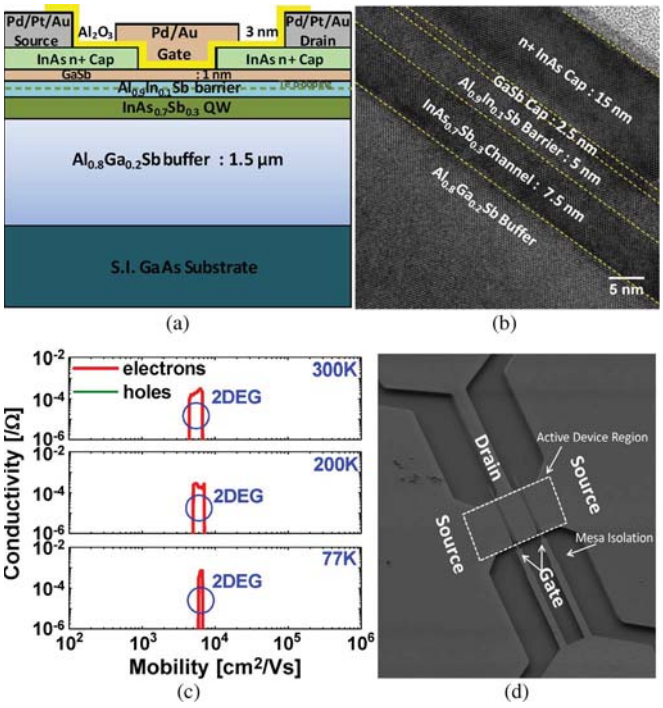

Fig. 1. (a) Schematic of the QW device structure. (b) TEM image of an $InAs_{0.7}Sb_{0.3}$ QW stack with a GaSb cap. The GaSb cap enables dielectric integration [4], and the n^+ InAs cap is used to improve access resistance. (c) QMSA of $InAs_{0.7}Sb_{0.3}$ QW heterostructure layers showing single dominant electron conductivity peak, indicating no parallel conduction in the barrier or buffer layer. (d) Top-view SEM image of the $InAs_{0.7}Sb_{0.3}$ QW MOSFET with $L_G = 150$ nm.

liftoff process. The devices received a 10-min postdeposition anneal at 180 °C in a N_2 ambient to densify the dielectric and reduce the interface and bulk defects.

III. DC and AC Characterization

Fig. 2(a) shows the effect of N_2 anneal on the transfer characteristics of the fabricated device. Subthreshold slope (SS) improves to 150 mV/dec after anneal from 310 mV/dec before anneal, whereas the gate leakage reduces by ∼400× after anneal. Fig. 2(b) shows the output characteristics of $L_G = 5$ μm devices, which shows excellent saturation without any effect of impact ionization. High drain-to-source ON-current of 40 μA/μm is obtained for the $L_G = 5$ μm device at drain bias of 0.5 V. The short-channel devices, however, suffer from high access resistance (from the undercut of the InAs cap), which limits the ON-current. Fig. 2(c) shows the split C–V characteristics of the thin QW device with 3 nm Al_2O_3−1nm GaSb at 77 K and 300 K, respectively. The interface state density in these devices is 6×10^{12} cm$^{-2} \cdot$ eV^{-1} obtained from the conductance analysis. Fig. 3(a) shows the effective electron drift mobility as a function of N_s. The interface charge contribution to the total charge density is corrected using split and simulated C–V [6], [7]. Record high effective electron drift mobility of 5200 cm^2/V $\cdot$ s was achieved at N_s of 1.8×10^{12} cm^{-2}, which is close to the Hall mobility of 5500 cm^2/V $\cdot$ s at the same N_s. The effective electron drift mobility as a function of the capacitive equivalent thickness (CET) is shown in Fig. 3(b). A 2.5× improvement in mobility was obtained

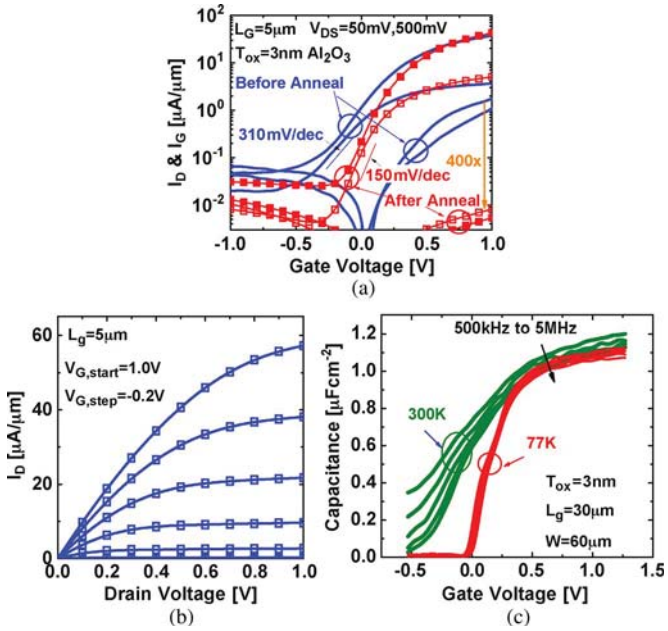

Fig. 2. (a) Transfer characteristics of the $L_G = 5$ μm device. (b) Output characteristics of the $L_G = 5$ μm device, showing very good saturation without any effect of impact ionization. (c) Split C–V characteristics at 77 K and 300 K.

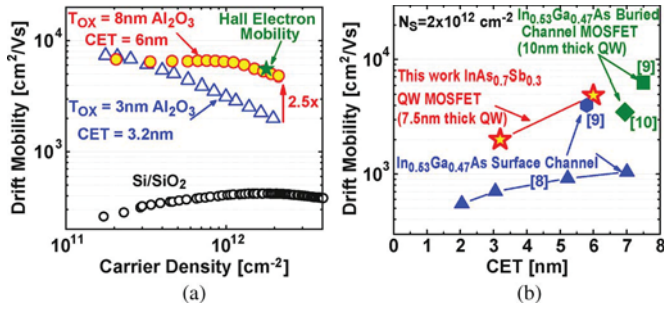

Fig. 3. (a) Effective electron drift mobility as a function of carrier density showing 2.5× enhancement on scaling oxide thickness. Record high electron mobility of 5200 cm^2/V $\cdot$ s achieved for the device with an 8-nm oxide at $N_s = 1.8 \times 10^{12}$ cm^{-2}. (b) Effective electron drift mobility as a function of CET for the thin QW device (CET is obtained from split C–V, and it includes semiconductor capacitance).

from increasing the oxide thickness from 3 to 8 nm, indicating that the dominant scattering mechanism is due to fixed charge at the Al_2O_3−GaSb or metal−Al_2O_3 interface.

IV. RF Characterization

Limited data exist in literature to date on high-frequency characterization of III–V QWFETs with integrated high-κ dielectric. RF characterization allows extraction of the intrinsic device metrics (C_{gs}, C_{gd}, g_m, g_{ds}, v_{eff}, and f_t) and the parasitic resistive and capacitive elements limiting the short-channel device performance. The S-parameters of the device under test and the open and short dummy structures are measured. The S-parameters of the device are obtained after the open–short deembedding to remove the parasitic resistance and capacitance. From the deembedded S-parameters of the device, C_{gs}, C_{gd}, g_m, and g_{ds} are obtained. Fig. 4(a) shows C_{gs}, C_{gd}, and C_{gg} as a function of frequency for devices with $L_G = 150$ nm and 1 μm. The deembedded S-parameters of

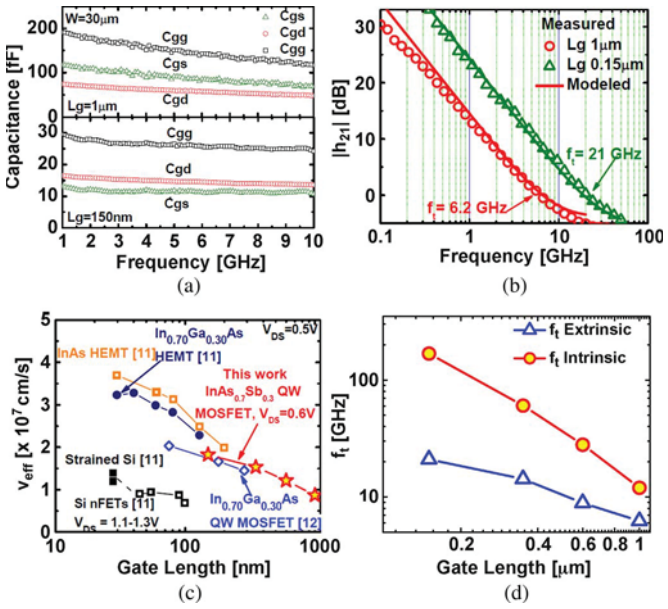

Fig. 4. (a) $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm gg}$ as a function of frequency for devices with $L_G = 150$ nm and 1 μm. High values of parasitic $C_{\rm gd}$ in these devices (due to incomplete isolation etch) limit RF performance, which could not be deembedded during the open calibration process. (b) Measured and modeled $|h_{21}|$ as a function of frequency. (c) Extracted intrinsic $v_{\rm eff}$ versus gate length showing $v_{\rm eff} = 1.8 \times 10^7$ cm/s for 150 nm L_G device, which is one of the highest effective velocities reported for III–V devices. (d) Intrinsic and extrinsic f_t versus gate length.

the device are modeled using an equivalent small-signal model to extract the intrinsic device parameters, using the evaluated $C_{\rm gs}$, $C_{\rm gd}$, g_m, and $g_{\rm ds}$. Fig. 4(b) shows the measured and the modeled $|h_{21}|$ versus frequency for $L_G = 150$ nm device (extrinsic $f_t = 21$ GHz) and $L_G = 1$ μm device (extrinsic $f_t = 6.5$ GHz) from 100 MHz to 20 GHz, which provides an excellent fit. High values of parasitic $C_{\rm gd}$ in these devices (due to incomplete isolation etch) limit the RF performance, which could not be deembedded during the open calibration process. For the 150-nm L_G device, $C_{\rm gd}$ exceeds $C_{\rm gs}$, which limits effective velocity $v_{\rm eff}$ and cutoff frequency f_t.

Fig. 4(c) shows the extracted source injection velocity ($v_{\rm eff} = g_{\rm mi}/$slope ($C_{\rm gs}$ versus L_G), where $g_{\rm mi}$ is the intrinsic transconductance of the device) for different gate length devices. The device with 150 nm L_G has a $v_{\rm eff}$ of 1.8×10^7 cm/s, which is one of the highest reported for III–V MOSFETs. Fig. 4(d) shows the intrinsic and extrinsic f_t versus L_G ($f_t = v_{\rm eff}/2\pi L_G$). The intrinsic f_t is 160 GHz for the 150-nm device and 12 GHz for the 1-μm device.

V. Conclusion

E-mode $InAs_{0.7}Sb_{0.3}$ QW MOSFETs have been demonstrated for the first time with record high effective electron drift mobility of 5200 $\rm cm^2/V \cdot s$ at N_s of 1.8×10^{12} $\rm cm^{-2}$, subthreshold slope of 150 mV/dec, and $I_{\rm ON}/I_{\rm OFF}$ ratio of $\sim$4000$\times$ within a voltage window of $\sim$1 V. A record high short-channel electron velocity of 1.8×10^7 cm/s (after series resistance correction) and intrinsic f_t of 160 GHz (extrinsic f_t of 21 GHz, limited by parasitic capacitance and resistance) are reported in a 150-nm L_G device, for the first time.

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